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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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INTEGRATED CIRCUITRY AND METHODS OF FORMING CIRCUITRY

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INTEGRATED CIRCUITRY AND METHODS OF FORMING CIRCUITRY

TECHNICAL FIELD

This invention pertains to semiconductive processing methods of forming integrated circuitry, as well as to semiconductive device circuitry.

BACKGROUND OF THE INVENTION

A common method of forming memory devices is to form an array of devices (a so-called memory array), and to form control devices at a periphery of the array. The memory array can comprise, for example, a dynamic random access memory (DRAM) array comprising arrays of capacitors and transistors. The peripheral circuitry can comprise, for example, transistors. Frequently, the memory array circuitry and the peripheral circuitry will be covered by insulative materials. Conductive contact plugs can be formed to extend through the insulative materials to electrically connect peripheral circuitry and memory array circuitry to one another, or to other circuitry.

A continuing goal in semiconductor device fabrication is to minimize process steps. Accordingly, it would be desired to develop processing methods which reduce processing steps associated with forming memory array circuitry and peripheral circuitry.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming circuitry. A capacitor electrode is formed over one region of a substrate and a conductive diffusion barrier layer is formed proximate the electrode. A dielectric layer is formed. The diffusion barrier layer is between the electrode and the dielectric layer. A conductive plug is formed over another region of the substrate. The conductive plug comprises a same material as the conductive diffusion barrier layer and at least a portion of the conductive plug is formed simultaneously with the conductive diffusion barrier layer.

In another aspect, the invention encompasses an integrated circuit comprising a capacitor and a conductive plug wherein the conductive plug and capacitor include a common and continuous layer.

In yet another aspect, the invention encompasses a circuit construction. The circuit construction includes a substrate having a memory array region and a region that is peripheral to the memory array region. The circuit construction also includes a capacitor construction over the memory array region of the substrate. The capacitor construction comprises a storage node, a dielectric layer and a cell plate layer. The dielectric layer is between the storage node and the cell plate layer. The circuit construction further includes an electrical interconnect over the peripheral region. The interconnect is

electrically connected to the cell plate layer and extends between the cell plate layer and the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a fragmentary, diagrammatic, cross-sectional view of a semiconductive wafer fragment at a preliminary processing step of a method of the present invention.

Fig. 2 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 7.

Fig. 9 is a view of the Fig. 1 wafer fragment shown at a step subsequent to that of Fig. 6 in accordance with a second embodiment method of the present invention.

Fig. 10 is a view of the Fig. 9 wafer fragment shown at a step subsequent to that of Fig. 9.

Fig. 11 is a view of the Fig. 1 wafer fragment shown at a step subsequent to that of Fig. 3 in accordance with a third embodiment method of the present invention.

Fig. 12 is a view of the Fig. 11 wafer fragment shown at a processing step subsequent to that of Fig. 11.

Fig. 13 is a view of the Fig. 1 wafer fragment shown at a processing step subsequent to that of Fig. 6 in accordance with a fourth embodiment method of the present invention.

Fig. 14 is a view of a semiconductive wafer fragment shown at a processing step subsequent to that of Fig. 2 in accordance with a fifth embodiment method of the present invention.

Fig. 15 is a view of the Fig. 14 wafer fragment shown at a processing step subsequent to that of Fig. 14.

Fig. 16 is a view of the Fig. 14 wafer fragment shown at a processing step subsequent to that of Fig. 15.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In one aspect, the present invention encompasses a recognition that processing steps associated with the formation of circuitry over a memory array region of a semiconductive wafer substrate can be consolidated with processing steps associated with formation of circuitry over a peripheral region of the substrate. Such will become more apparent with reference to Figs. 1-6, which illustrate initial processing of a method of the present invention.

Referring initially to Fig. 1, a semiconductor wafer fragment 10 comprises a semiconductive substrate 12. Substrate 12 can comprise, for example, a monocrystalline silicon wafer lightly doped (i.e., doped to a concentration of less than or equal to about 10^{16} atoms/cm^3) with a p-type dopant. To aid in interpretation of the claims that follow, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described

above. Semiconductive substrate 12 comprises a memory array region 14 and a peripheral region 16.

Word lines 18, 20 and 22 are formed over substrate 12. Word lines 18, 20 and 22 comprise a gate stack 24 and sidewall spacers 26. Gate stack 24 can comprise, for example, layers of silicon dioxide, polysilicon and silicide. Sidewall spacers 26 can comprise, for example, silicon nitride or silicon oxide.

Field oxide regions 28 are formed over substrate 12 within memory array region 14. Field oxide regions 28 can comprise, for example, silicon dioxide.

Electrical nodes 30 and 32 are defined adjacent word line 18, and electrical nodes 34, 36 and 38 are defined adjacent word lines 20 and 22. Wordlines 18, 20 and 22 can comprise transistors, and nodes 30, 32, 34, 36 and 38 can comprise source/drain regions of such transistors. Nodes 30 and 32 are proximate peripheral region 16 of substrate 12. The term "proximate" indicates that nodes 30 and 32 can be within, above or below peripheral region 16 of substrate 12 (embodiments in which nodes are elevationally displaced from substrate 12 are not shown). Similarly, nodes 34, 36 and 38 are proximate memory array region 14 of substrate 12. Nodes 30, 32, 34, 36 and 38 can comprise, for example, conductive diffusion regions formed within substrate 12. Such diffusion regions can be formed by, for example, implanting conductivity-enhancing dopant into substrate 12.

An electrically insulative layer 40 is formed over substrate 12, and over word lines 18, 20 and 22. Insulative layer 40 can comprise, for example, borophosphosilicate glass (BPSG), and can be formed by, for example, chemical vapor deposition.

Referring to Fig. 2, openings 42 and 44 are etched through insulative layer 40 to nodes 34 and 38, respectively. Openings 42 and 44 can be formed by, for example, providing a photoresist mask (not shown) over layer 40, and patterning the mask to expose regions of insulative layer 40 at opening locations 42 and 44. Insulative layer 40 can then be etched with, for example, a fluorine-containing plasma to form openings 42 and 44. The photoresist mask can be subsequently removed to leave the structure shown in Fig. 2.

Referring to Fig. 3, capacitor storage nodes 46 and 48 are formed within openings 42 and 44 (Fig. 2), respectively. Capacitor storage nodes 46 and 48 can comprise, for example, polysilicon and preferably comprise the shown roughened outer surfaces 50 and 52. Such roughened outer surfaces can be formed by, for example, deposition of hemispherical grain polysilicon.

A dielectric layer 54 is formed over storage nodes 46 and 48. Dielectric layer 54 can comprise, for example, one or more of silicon dioxide or silicon nitride, and preferably comprises tantalum oxide. Dielectric layer 54 can be formed by, for example, chemical vapor deposition. Storage nodes 46 and 48, and dielectric layer 54, can be

formed by methods known to persons of ordinary skill in the art, such as, for example, chemical vapor deposition. In the shown embodiment, the material of storage nodes 46 and dielectric layer 54 does not extend over peripheral region 16. Such can be accomplished by, for example, masking peripheral region 16 while forming nodes 46 and 48, and while forming dielectric layer 54.

Referring to Fig. 4, a photoresist masking layer 56 is provided over regions 14 and 16 of substrate 12 and patterned to define openings 58 and 60 in peripheral region 16.

Referring to Fig. 5, openings 58 and 60 are extended to node locations 30 and 32, respectively. Openings 58 and 60 can be extended by, for example, a plasma etch utilizing a fluorine-containing component.

Referring to Fig. 6, photoresist material 56 (Fig. 5) is removed. Subsequently, a conductive material 62 is formed over both peripheral region 16 and memory array region 14 of substrate 12. In the shown embodiment, conductive material 62 comprises two separate layers (64 and 66). Layer 64 can comprise, for example, a metal nitride, such as titanium nitride or tungsten nitride, and layer 66 could comprise a metal such as tungsten, aluminum or copper. The metal of layer 66 can be in either an elemental form, or in the form of an alloy, such as aluminum/copper. Layers 64 and 66 can be formed by, for example, chemical vapor deposition and/or sputter deposition.

Layers 64 and 66 would typically have different functional purposes at peripheral region 16 relative to memory array region 14. Specifically, layers 64 and 66 form contact plugs 65 and 67 at peripheral region 16, with layer 64 preferably comprising a metal nitride and functioning as an adhesive layer for adhering metal layer 66 within openings 58 and 60 (Fig. 5). Layer 64 can also function to prevent diffusion of dopant from diffusion regions 30 and 32 into metal layer 66. In contrast, layers 64 and 66 form at least a portion of a capacitor electrode 81 over memory array region 14. Specifically, layers 64 and 66 together define at least a portion of capacitor cell plate 81, with conductive material 62 and dielectric layer 54 being operatively adjacent storage node layers 46 and 48 to form capacitor structures 70 and 72. In embodiments in which dielectric layer 54 comprises tantalum oxide, layer 64 preferably comprises a metal nitride. Layer 64 can then function as a capacitor diffusion barrier layer to inhibit undesired diffusion of materials between tantalum oxide layer 54 and upper capacitor electrode layer 66.

Although material 62 is shown as comprising two layers, it is to be understood that the invention also encompasses embodiments in which material 62 comprises only one layer, and other embodiments in which material 62 comprises more than two layers. For instance, material 62 can comprise three layers wherein a first layer is titanium deposited to form titanium silicide at the bottoms of openings 58 and 60 (Fig. 5),

and the remaining two layers are a metal nitride layer (such as TiN) and a metal layer (such as Al).

In the shown embodiment, conductive material layer 62 is formed over peripheral region 16 and memory array region 14 in a common deposition step. Thus, such embodiment consolidates formation of conductive contact plugs 65 and 67 with formation of capacitor electrode 81 over memory array region 14. Such can save process steps relative to prior art methods which form conductive contacts over a peripheral region of a substrate separately from formation of a capacitor electrode over a memory array region of the substrate.

Figs. 7-10 illustrate alternative processing methods which can be utilized for patterning conductive material at peripheral region 16. Figs. 7-8 illustrate a first embodiment method, and Figs. 9-10 illustrate a second embodiment method. Referring first to the embodiment of Figs. 7 and 8, and specifically referring first to Fig. 7, a photoresist masking layer 76 is provided over memory array region 14 while leaving peripheral region 16 exposed to an etching process. The etch process removes conductive material 62 from over insulative material 40 at peripheral region 16 to electrically isolate conductive plugs 65 and 67 from one another.

Referring to Fig. 8, a conductive layer 80 is formed over memory array region 14 and peripheral region 16 and patterned to form isolated electrical contacts with conductive plugs 65 and 67, and to form another

portion of capacitor electrode 81 for capacitor constructions 70 and 72. More specifically, layer 80 and conductive material 62 together form capacitor electrode 81 for capacitors 70 and 72. Conductive layer 80 can comprise, for example, a metal such as tungsten, titanium, copper and/or aluminum, and can be formed by, for example, sputter deposition. Alternatively, conductive layer 80 can comprise a conductively doped semiconductive material, such as, for example, conductively doped polysilicon. Subsequent processing (not shown) such as provision of an interlevel dielectric or spin-on-glass over one or both of regions 14 and 16, followed by chemical-mechanical planarization can be conducted to form an insulative layer over regions 14 and 16.

Referring to the embodiment of Figs. 9 and 10, identical numbering to that utilized in describing the embodiment of Figs. 7 and 8 will be used. A difference between the embodiment of Figs. 9 and 10 and that of Figs. 7 and 8 is that in the Fig. 9 and 10 embodiment conductive material 80 is formed over memory array region 14 and peripheral region 16 prior to etching of conductive material 62.

Referring initially to Fig. 9, conductive layer 80 has been formed over memory array region 14 and peripheral region 16.

Referring to Fig. 10, conductive layer 80 and conductive material 62 are patterned in a common etch to electrically isolate conductive plugs 65 and 67 from one another, and to electrically isolate the circuitry of peripheral region 16 from that of memory array

region 14. The patterning of material 62 and layer 80 can comprise, for example, formation of a patterned photoresist layer (not shown) over layer 80, and subsequent transferring of a pattern from the photoresist layer to underlying layer 80 and conductive material 62 to form the structure shown in Fig. 10. The patterned photoresist layer forms a protective layer over a portion of conductive material 80 that is over storage nodes 46 and 48 that protects such portion of conductive material 80 as another portion of conductive material 80 is removed from over peripheral region 16. The portion of conductive material 80 removed from peripheral region 16 is proximate to where openings 58 and 60 (Fig. 5) were formed.

Another embodiment of the invention is described with reference to Figs. 11 and 12. In describing to Figs. 11 and 12, identical numbering to that utilized above in describing Figs. 1-10 will be used, with differences indicated by different numerals.

Referring first to Fig. 11, semiconductive wafer fragment 10 is shown at a processing step subsequent to that of Fig. 3, with a layer 90 formed over dielectric layer 54 in memory array region 14, and extending to over peripheral region 16. Layer 90 can comprise, for example, a diffusion barrier layer such as, for example, titanium nitride or tungsten nitride.

Referring to Fig. 12, openings are formed through layer 90 and to node locations 30 and 32, and subsequently filled with conductive

material 62. The formation of the openings and subsequent filling of such openings with conductive material 62 can occur through processing similar to that described with reference to Figs. 4-6. Wafer fragment 10 of Fig. 12 can then be subjected to subsequent processing analogous to that of either the embodiment of Figs. 7-8 or the embodiment of Figs. 9-10 to form isolated conductive plugs in electrical contact with node locations 30 and 32, and to form capacitor structures similar to the structures 70 and 72 of Figs. 8 and 10.

Yet another embodiment of the present invention is described with reference to Fig. 13 which illustrates a semiconductive wafer fragment 10 at a processing step subsequent to that of Fig. 9. In the Fig. 13 embodiment, conductive layer 80 and conductive material 62 are patterned to electrically isolate contact plugs 65 and 67 from one another, but contact plug 67 remains in electrical connection with the upper capacitor electrode 81 over memory array region 14. Thus layers 64 and 66 are common and continuous layers comprised by both contact plug 67 and capacitors 70 and 72. In the Fig. 13 embodiment, contact plug 67 forms an electrical connection between memory array region 14 and electrical node 32.

The embodiment of Fig. 13 can be advantageous over prior art methods for providing a good electrical contact to a cell plate electrode. Specifically, prior art methods utilize electrical connects extending upwardly from a cell plate layer. Such electrical connects are formed

by providing an insulative layer over the cell plate layer and etching downwardly through the insulative layer to expose the cell plate layer. Occasionally, the etch extends through the cell plate layer and results in a poor electrical connection to the cell plate layer. In contrast, the embodiment of Fig. 13 utilizes an electrical connection extending downwardly from a cell plate layer and formed during formation of the cell plate layer. Specifically, at least a portion of the cell plate layer 81 is preferably formed over electrical interconnect 67 during formation of electrical interconnect 67.

It is noted that the invention also encompasses embodiments wherein cell plate layer 81 from memory array region 14 extends to physically contact more than one contact plug in peripheral region 16. Such embodiments can provide redundancy in the event that one or more of the connections fails. In the shown embodiment, interconnects 65 and 67 are connected through a switch comprising word line 18. Interconnect 65 can then be connected to other circuitry (not shown) to provide a switchable connection between such other circuitry and the capacitor plate 81 over memory region 14.

Yet another embodiment of the present invention is described with reference to Figs. 14-16. In describing the embodiment of Figs. 14-16, identical numbering to that utilized above in describing the embodiments of Figs. 1-13 will be used, with differences indicated by different numerals.

Referring to Fig. 14, wafer fragment 10 is illustrated at a processing step subsequent to that of Fig. 2. Specifically, storage nodes 46 and 48 are formed within openings 42 and 44 (Fig. 2). Wafer fragment 10 of Fig. 14 differs from the wafer fragment 10 of Fig. 3 (which is also at processing step subsequent to that of Fig. 2) in that there is no dielectric layer 54 provided over storage nodes 46 and 48 in the embodiment of Fig. 14.

Fig. 15 illustrates the wafer fragment 10 of Fig. 14 after it has been subjected to processing analogous to that described above with reference to Figs. 4-6. Specifically, a conductive material 62 has been formed over storage nodes 46 and 48. Conductive material 62 has also been formed in electrical contact with node locations 32 to form electrical interconnects 65 and 67 over peripheral region 16 of substrate 12. As there was no dielectric layer formed prior to provision of conductive material 62, material 62 electrically interconnects with nodes 46 and 48 to effectively become a portion of the capacitor storage nodes 46 and 48.

A patterned photoresist layer 100 is provided over peripheral region 16 and memory array region 14. Patterned photoresist layer 100 has openings 102 extending through it.

Referring to Fig. 16, openings 102 (Fig. 15) are extended to electrically isolate electrical interconnects 65 and 67 from one another and from memory array region 14, as well as to electrically isolate

storage nodes 46 and 48 from one another. Photoresist layer 100 (Fig. 15) is then removed, and a dielectric layer 54 is formed over memory array region 14. Dielectric layer 54 can be formed by, for example, processing described above with reference to Fig. 3. After formation of dielectric layer 54, a conductive layer 80 is provide over storage nodes 46 and 48, as well as over electrical interconnects 65 and 67. Conductive material 80 is then patterned to form a cell plate 81 over storage nodes 46 and 48, and to form electrically isolated contacts to interconnects 65 and 67. The formation and patterning of layer 80 can be conducted in accordance with the methods described above in reference to Figs. 7 and 8.

The embodiment of Figs. 14-16 forms a diffusion barrier layer 64 that is part of capacitor storage nodes 46 and 48. In the shown embodiment, material 62 can comprise diffusion barrier components throughout its thickness. Specifically, layers 64 and 66 can both comprise either titanium nitride or tungsten nitride.

It is noted that the embodiments described above form a diffusion barrier layer as either part of a storage node, or as a part of a capacitor plate. The invention encompasses other embodiments (not shown) wherein one or more of the above-described embodiments are combined to form a diffusion barrier region as part of a storage node and to also form a diffusion barrier region as part of a capacitor plate.

It is also noted that there will typically be a bit line contact (not shown) formed in electrical connection with node 36 in the embodiments described above to connect node 36 to a bit line (not shown). Such bit line can be either above the capacitors (a so-called capacitor over bit line construction) or beneath at least a portion of the capacitors (a so-called capacitor over bit line construction).

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.